

Substitute Form PTO-1449 (Modified) U.S. Department of Commerce Patent and Trademark Office Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR 1.98(b))	Attorney's Docket No. 10559-618001	Application No. 10/057,738
	Applicant Gilbert Wolrich et al.	
	Filing Date 01/25/2002	Group Art Unit 2187

U.S. Patent Documents


Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
N	AA	09/475,614	12/30/1999	Wolrich et al.			
N	AB	09/473,571	12/28/1999	Wolrich et al.			

Foreign Patent Documents or Published Foreign Patent Applications

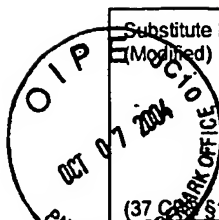
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
N	AC	WO 01/50679	07/12/2001	WIPO				
	AD	WO 01/50247	07/12/2001	WIPO				
	AE	WO 01/48619	07/05/2001	WIPO				
	AF	WO 01/48606	07/05/2001	WIPO				
	AG	WO 01/48596	07/05/2001	WIPO				
	AH	WO 01/16782	03/08/2001	WIPO				
	AI	WO 01/16770	03/08/2001	WIPO				
	AJ	WO 01/16769	03/08/2001	WIPO				
	AK	WO 01/15718	03/08/2001	WIPO				
	AL	WO 97/38372	10/16/1997	WIPO				
	AM	WO 94/15287	07/07/1994	WIPO				
	AN	EP 0 809 180	11/26/1997	Europe				
	AO	EP 0 745 933	12/04/1996	Europe				
	AP	EP 0 633 678	01/11/1995	Europe				
	AQ	EP 0 464 715	01/08/1992	Europe				
	AR	EP 0 379 709	08/01/1990	Europe				
N	AS	59-111533	06/27/1984	Japan (with English Abstract)				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
N	AT	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
N	AU	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 nd ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.

Examiner Signature 	Date Considered 01/03/05
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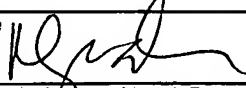
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	Information Disclosure Statement by Applicant (Use several sheets if necessary)			Applicant Gilbert Wolrich et al.
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Other Documents (include Author, Title, Date, and Place of Publication)

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ND	AV	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
	AW	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
	AX	"HART, Field Communications Protocol, Application Guide", 'Online! 1999, Hart Communication Foundation, Austin, TX, XP002219606, http://lhc-div.web.cern.ch/lhc-div/IAS/WS/WorldFip/Labo/appguide.pdf
	AY	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
	AZ	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.
	AAA	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225.
	ABB	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55.
	ACC	Romilly Bowden, "What is HART?," Romilly's Hart and Fieldbus Web Site, Online!, 1977, XP002219605, http://www.romilly.co.uk/whathart.htm
	ADD	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online!</i> , 13 November 1998.
	AEE	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
	AFF	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28 th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
	AGG	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1998.
	AHH	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , 18 March 1999.
	AII	Vibhatavani et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359.
ND	AJJ	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.
	AKK	
	ALL	
	AMM	
	ANN	
	AOO	

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